CLAIMS

Claim 1. A method of calibrating RC time constant of an RC filter using a differential amplifier with a coupling capacitor C between each output terminal and each input terminal of the differential amplifier and a resistor R between each input terminal and each input reference signal, comprising the steps of:

using a first calibration cycle; and

using a second calibration cycle to cancel the offset error of the differential amplifier.

Claim 2. The method of calibrating RC time constant as described in claim 1,

wherein the first calibration cycle uses as a first input reference signal, which is the sum of a common mode voltage Vcm and a first reference voltage Vref1, and a second input reference signal, which is the difference of Vcm minus a second reference voltage Vref2, to said differential amplifier to generate a first dual-slope ramp signal;

wherein the second calibration cycle repeats the first calibration cycle but using a reverse input reference signals to the differential amplifier to generate a second dual-slope ramp signal, and

wherein the time slots for the first and second dual-slope ramp signals to reverse ramping direction and cross zero are used to calibrate the value of the capacitance of the RC time constant.

Claim 3. The method of calibrating RC time constant of an RC filter as described in claim 2, wherein said first calibration cycle and said second calibration cycle comprise the steps of:

pre-loading a predefined number to a (N+1)-bit counter;

generating a control signal *PhA* for a first fixed time duration which comprises sub-duration 1, sub-duration 2, and sub-duration 3,

wherein sub-duration 1 is an auto-zeroing duration, during which a control signal *PhB* is generated to short-circuit a feedback capacitor C_{0a} between an inverting input and non-inverting output of said differential amplifier through a first series input programmable resistor R_{1a} connected between said inverting input and said first input reference signal, and to short-circuit a feedback capacitor C_{0b} between a non-inverting input and inverting output of said differential amplifier through a second series input programmable resistor R_{1b} connected between said non-inverting input and said second input reference signal,

wherein a control signal *PhC* is generated for said sub-duration 2 such that the first input reference signal charges said C_{0a} through said R_{1a}, and the second input reference signal charges said C_{0b} through said R_{1b},

wherein control signals *PhD*, Φ_D and $\overline{\Phi_D}$ are generated for said sub-duration 3 such that said C_{0a} is discharged through a first switched capacitor equivalent resistor with capacitor C_{1a} switched by clocks Φ_D and $\overline{\Phi_D}$ and said C_{0b} is discharged through a second switched capacitor equivalent resistor with capacitor C_{1b} switched by clocks Φ_D and $\overline{\Phi_D}$;

generating a control signal $\overline{PhA}$ for a second fixed time duration which comprises sub-duration 4, sub-duration 5, and sub-duration 6,

wherein sub-duration 4 is an auto-zeroing duration [of the differential amplifier], during which said control signal *PhB* is generated to short-circuit the individual two ends of said C_{0a} and C_{0b},

wherein said control signal *PhC* is generated for said sub-duration 5 such that the second input reference signal charges said C_{0a} through said R_{1a} and the first input reference signal charges said C_{0b} through said R_{1b},

wherein said control signals *PhD*, Φ_D and $\overline{\Phi_D}$ are generated for said sub-duration 6 such that said C_{0a} is discharged through said first switched capacitor equivalent resistor with capacitor C_{1a} switched by clocks Φ_D and $\overline{\Phi_D}$ and said C_{0b} is discharged through said second switched capacitor equivalent resistor with capacitor C_{1b} switched by clocks Φ_D and $\overline{\Phi_D}$;

generating a first duration η_1 when the difference of the non-inverting output and the inverting output of said differential amplifier reverses ramping direction and crosses zero in said sub-duration 3;

generating a second duration η_2 when the difference of the non-inverting output and the inverting output of said differential amplifier reverses ramping direction and crosses zero in said sub-duration 6;

enabling said (N+1)-bit counter during the periods of η_1 and η_2; and

outputting from said (N+1)-bit counter the most significant N-bit count as a signal to set the capacitor array capacitance of an RC filter.

Claim 4. The method of calibrating RC time constant of an RC filter as described in claim 1, wherein the said RC filter is selected from the group consisting of: a low-pass, band-pass, high-pass, single and multiple order filter with resistors and capacitor arrays constituting RC time constant to be calibrated.

Claim 5. The method of calibrating RC time constant of an RC filter as described in claim 3, wherein said capacitor array is binary-weighted.

Claim 6. The method of calibrating RC time constant of an RC filter as described in claim 3, wherein said capacitor array is fed from a digital counter.

Claim 7. The method of calibrating RC time constant of an RC filter as described in claim 3, wherein a different calibration reference clock rate is used, further comprising the step of:

pre-setting the resistance of said programmable resistors R_{1a} and R_{1b} in claim 3 according to the ratio of the new reference clock period to the original based reference clock period.

Claim 8. The method of calibrating RC time constant of an RC filter as described in claim 3, wherein the filter default cut-off frequency is changed, further comprising the step of:

pre-setting the resistance of said programmable resistors R_{1a} and R_{1b} in claim 3 according to the ratio of the new filter cut-off frequency to the default filter cut-off frequency.

Claim 9. The method of calibrating RC time constant of an RC filter as described in claim 3, wherein a different calibration reference clock rate is used and the filter default cut-off frequency is changed, further comprising the step of:

pre-setting the resistance of said programmable resistors R_{1a} and R_{1b} in claim 3 according to the ratio of the new reference clock period to the original based reference clock period times the ratio of the new filter cut-off frequency to the default filter cut-off frequency.

Claim 10. The method of calibrating RC time constant of an RC filter as described in claim 3, further comprising the step of running the steps of claim 3 multiple times.

Claim 11. The method of calibrating RC time constant as described in claim 3, wherein said RC filter is a passive filter.

Claim 12. The method of calibrating RC time constant as described in claim 3, wherein said RC filter is an active filter.

Claim 13. A variable rate RC calibration circuit comprising:

a differential amplifier with a first capacitor C_{0a} between the inverting input and the non-inverting output of said differential amplifier and a second capacitor C_{0b} between the non-inverting input and the inverting output of said differential amplifier;

first input programmable resistor R_{1a} to said inverting input and second programmable resistor R_{1b} to said non-inverting input of said differential amplifier,

first switched capacitor equivalent resistor with capacitor a C_{1a} to said inverting input, and second switched capacitor equivalent resistor with a capacitor C_{1b} to said non-inverting input of said differential amplifier, and

calibration signals of calibrating $R_{1a}C_{1a}$ time constant and $R_{1b}C_{1b}$ time constant in a first calibration cycle and a second calibration cycle to cancel the offset error of said differential amplifier.

Claim 14. The variable rate RC calibration circuit as described in claim 13, wherein the calibration signal of said first calibration cycle is a first dual-slope ramp signal and the calibration signal of said second calibration cycle is a second dual-slope ramp signal opposite to the first dual-slope ramp signal, and the time slots when the first and the second dual-slope ramp signals reverse ramping direction and cross zero are used to input a counter.

Claim 15. The variable rate RC calibration circuit as described in claim 14, wherein said time slot is quantized into steps and the number of steps are used to input the counter.

Claim 16. The variable rate RC calibration circuit as described in claim 15, wherein said time slot is quantized by discharging C_{0a} and C_{0b} through switched capacitor resistors during second halves of said first ramp signal and second ramp signal.